MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 3, 2021/2022

ECE4116 DIGITAL COMPUTER DESIGN

(All Section / Groups)

10 AUGUST 2022
9:00 a.m. – 11:00 a.m.
(2 hours)

INSTRUCTIONS TO STUDENT

1. This Question paper consists of 4 pages, including the cover page and with 4 Questions only.

2. Attempt **ALL** questions. All questions carry equal marks, and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

Question 1

(a) The Boolean function of the sum of the product (minimum terms) logic circuits is given as follows:

$F(a, b, c, d) = \sum m(0, 1, 2, 5, 6, 7, 15)$

(i) Draw the truth table for this logic circuit. [3 marks]

(ii) Implement the logic circuit by employing a 4-to-1 line multiplexer and appropriate logic gates. Connect input a and b to the selection line of the multiplexer. [6 marks]

(iii) Write a VHDL code for above-mentioned logic circuit [4 marks]

(b) A sequential circuit with two D flip-flops A and B, inputs Y and output Z is represented by the following input equation:

$$D_A = BY + \bar{A}Y, D_B = \bar{Y}, Z = \bar{A}\bar{B}$$

(i) Draw this sequential circuit. [4 marks]

(ii) Construct its state table. [4 marks]

(iii) Draw its state diagram. [4 marks]

Question 2

(a) Represent the following conditional control statements as two register transfer statements with control capabilities:

If (X=1) then ($R_1 \leftarrow R_2$) else if (Y=1) then ($R_1 \leftarrow R_3$) [5 marks]

(b) Design and draw a 1-bit logic diagram segment that implements the following instructions using two 4-bit registers, R1 and R2, and the appropriate logic gates.

C_0: $R_2 \leftarrow R_1$ Transfer R_1 to R_2

C_1: $R_2 \leftarrow \overline{R2}$ Complement R_2

C_2: $R_2 \leftarrow 0$ Clear R_2

The control variables are mutually exclusive (i.e., only one variable can be equal to 1 at any time) while the other two are equal to 0. [8 marks]

(c) A 64K×8 RAM will be constructed from multiple 16K×8 RAM chips.

(i) Determine the number of address lines available on each 16K×8 RAM chip. [2 marks]

(ii) Compute the number of address lines needed for the 64K×8 RAM [2 marks]

(iii) Draw the 64Kx8 RAM block diagram using 16K×8 RAM chips and a decoder. Show all address lines, data lines, and control inputs. [8 marks]

Continued...

Question 3

(a) An arithmetic circuit function table is shown in Figure Q3 (a). The inputs A and B are 16-bit data, and control signals $S0$ and $S1$. The output (F) is indicated as 16-bit value , F.

$S1$	$S0$	Function
0	0	$F = A$ (transfer)
0	1	$F = A + B$ (addition)
1	0	$F = A + \overline{B} + 1$ (subtraction)
1	1	$F = A + 1$ (increment)

Figure Q3(a)

The arithmetic circuit consists of a parallel adder with 2 data inputs, X and Y, an output, S, carry-in, Cin, and carry-out, $Cout$. Data A connects to X input, and data B connects to Y input. Y input requires additional logic to implement the functions given in Figure Q3a.

(i) Write the truth table for X, Y, and Cin input values in terms of A, B, $S0$, and $S1$. [4 marks]

(ii) Based on the truth table in (i), write the Boolean expressions for X, Y and Cin inputs. [3 marks]

(iv) Y input logic is implemented using a 4-to-1 multiplexer. Draw the complete circuit block diagram for the arithmetic circuit. [6 marks]

(b) A two-word instruction is stored in memory at an address designated by the symbol W. The symbol Y designates the address field of the instruction (stored at W+1). The operand used during the execution of the instruction is stored at the effective address symbolised by Z. An index register contains the value X. State how Z is calculated from the other addresses if the addressing mode of the instruction is:

(i) Direct. [2 marks]

(ii) Indirect. [2 marks]

(iii) Relative. [2 marks]

(iv) Indexed. [2 marks]

(c) A computer has a 32-bit word length; all instructions are one word in length with no mode field. The register file of the computer has 64 registers.

(i) For instruction with three register addresses and an 8-bit constant field, determine the maximum number of possible opcodes. [2 marks]

(ii) For an instruction format with two register addresses, one constant field and a maximum of 64 opcodes, what is the number of bits available for the constant field? [2 marks]

Continued...

Question 4

(a) A pipelined data path breaks the conventional data path into several parts using pipeline platforms in-between the parts.

(i) Describe how a pipelined data path results in faster execution than a conventional data path.

[2 marks]

(ii) A 4-stage pipeline will never achieve an improvement factor of 4. Describe the reason(s).

[4 marks]

(b) A hypothetical RISC machine employs a typical 4-stage pipeline. The following sequence of instructions is executed.

```
MOVA    R1, R5
SLT     R2, R4, R1
BNZ     R2, 25
MOVA    R5, R8
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(i) Draw the pipeline execution diagram to show the execution of the instructions. Subsequently, identify all hazards and specify what type they are?

[7 marks]

(ii) Describe the methods to resolve the hazards identified in part (i).

[6 marks]

(c) CISC machines have complex instructions, some of which require more than one execution cycle to complete. This characteristic makes it unsuitable for standard pipelining.

(i) Describe the modification that allows the implementation of a 4-stage pipeline for a CISC machine.

[2 marks]

(ii) Draw the block diagram to show the implementation.

[4 marks]

End of Paper